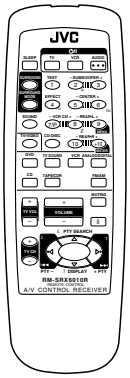
JVC

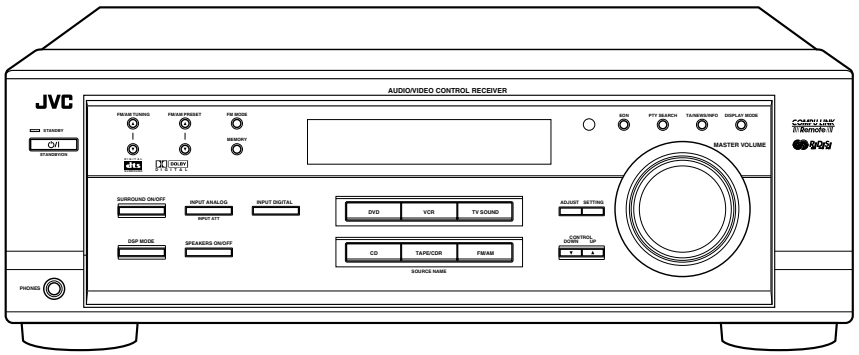
SERVICE MANUAL

AUDIO/VIDEO CONTROL RECEIVER

RX-6010RBK
RX-6012RSL

Area Suffix
RX-6010RBK
E ··· Continental Europe
EN ···· Northern Europe
RX-6010RSL
B ---------- U.K.
E ··· Continental Europe
EN ···· Northern Europe





As for RX-6012RSL the body is silver color

COMPU LINK Remote

DIGITAL dts SURROUND

DOLBY DIGITAL

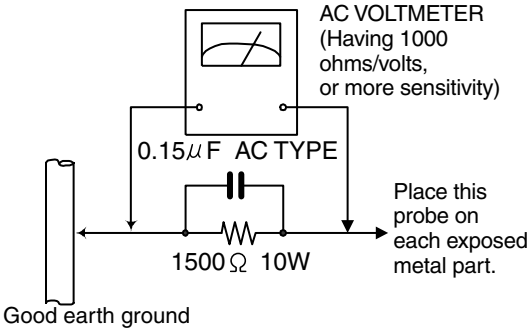
RIDISI

Contents

No.20932
Apr. 2001

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ CAUTION

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▮) and ICP (●) or identified by the "⚠" mark nearby are critical for safety.
When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the JC version)

Disassembly method

■ Removing the top cover (See Fig.1)

1. Remove the four screws A attaching the top cover on both sides of the body.
2. Remove the three screws B on the back of the body.
3. Remove the top cover from behind in the direction of the arrow while pulling both sides outward.

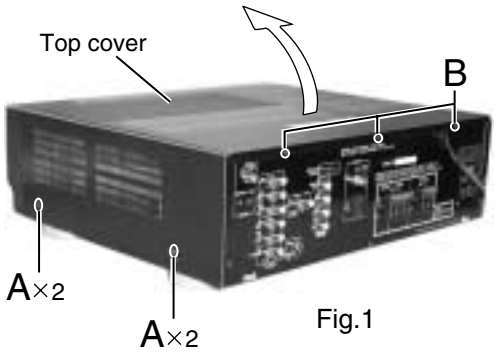


Fig.1

■ Removing the front panel assembly (See Fig.2 and 3)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from connector CN402 on the audio board and CN201 on the power supply board in the front panel assembly.
2. Cut off the tie band fixing the harness.
3. Remove the three screws C attaching the front panel assembly.
4. Remove the four screws D attaching the front panel assembly on the bottom of the body. Detach the front panel assembly toward the front.

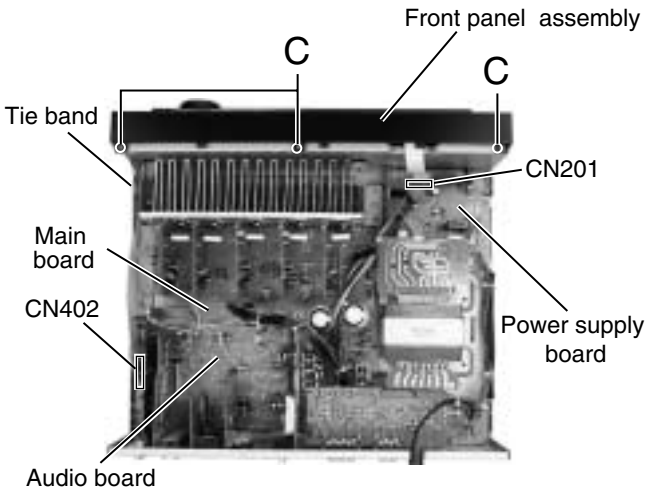


Fig.2

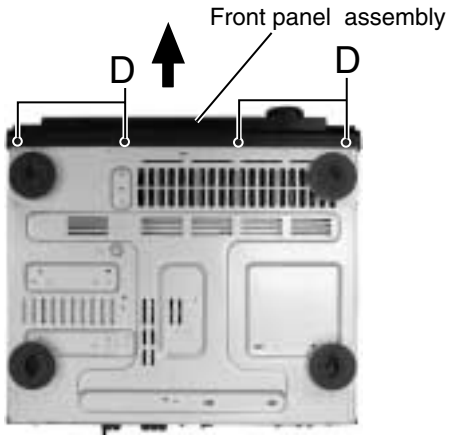


Fig.3

■ Removing the rear panel (See Fig.4)

- Prior to performing the following procedure, remove the top cover.

1. Remove the power cord stopper from the rear panel by moving it in the direction of the arrow.
2. Remove the seventeen screws E attaching the each boards to the rear panel on the back of the body.
3. Remove the four screws F attaching the rear panel on the back of the body.

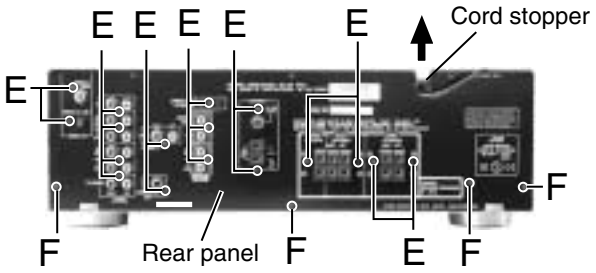


Fig.4

■ Removing each board connected to the rear side of the audio board

(See Fig.5 to 8)

- Prior to performing the following procedure, remove the top cover and the rear panel.

1. Cut off the tie band fixing the harness.
2. Disconnect the DSP board from connector CN481 on the audio board.
3. Disconnect the audio input board. DVD board and the video board from connector CN421, CN431 and CN441 on the audio board.
4. Disconnect the tuner board from connector CN411 and CN412 on the audio board.

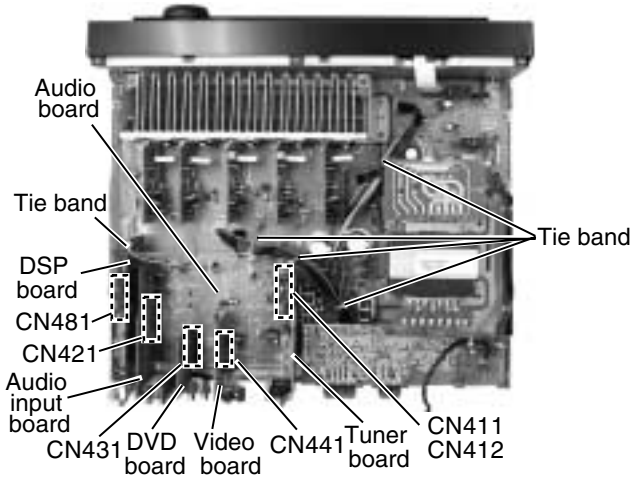


Fig.5

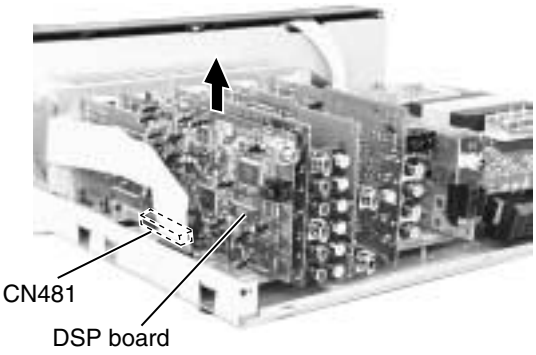


Fig.6

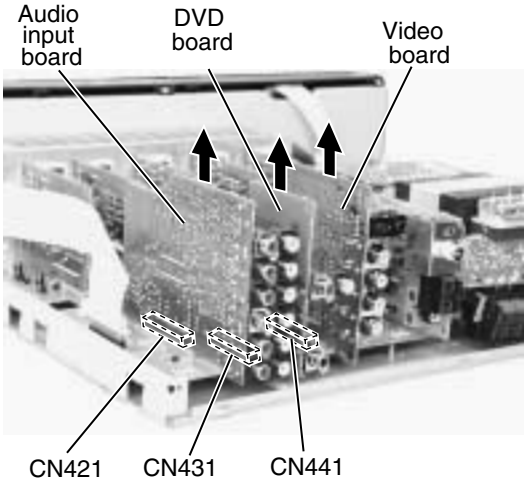


Fig.7

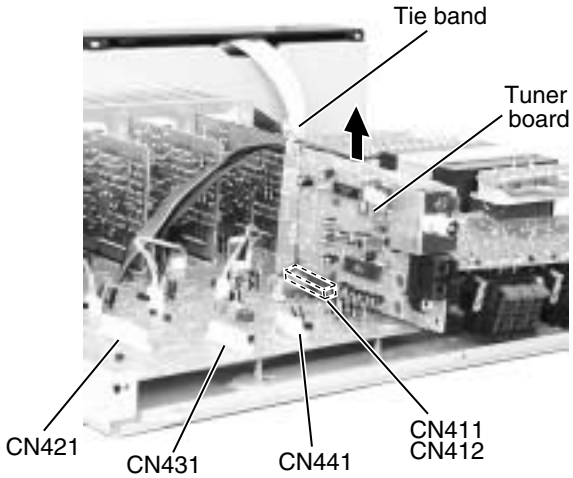


Fig.8

■Removing the audio board (See Fig.9)

・Prior to performing the following procedure, remove the top cover and the rear panel.

1. Disconnect the card wire from connector CN402 on the audio board.
2. Disconnect the relay board from the audio board and the power supply board. (CN291,CN491)
3. Disconnect the harness from connector CN473, CN471, CN472, CN403 and CN385.
4. Remove the three screws G attaching the audio board assembly.
5. Remove the screw H attaching the audio board assembly.

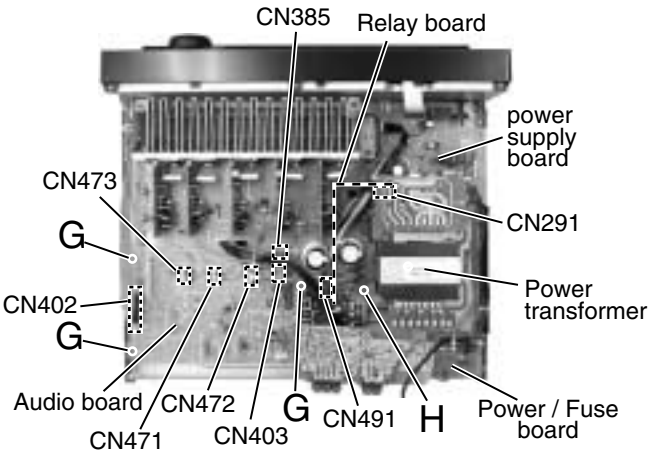


Fig.9

■Removing the main board. (See Fig.10)

・Prior to performing the following procedure, remove the top cover, the rear panel and audio board.

1. Disconnect the harness from connector CN241 and CN203 on the power supply board respectively.
2. Remove the four screws I and the two screws J attaching the main board.

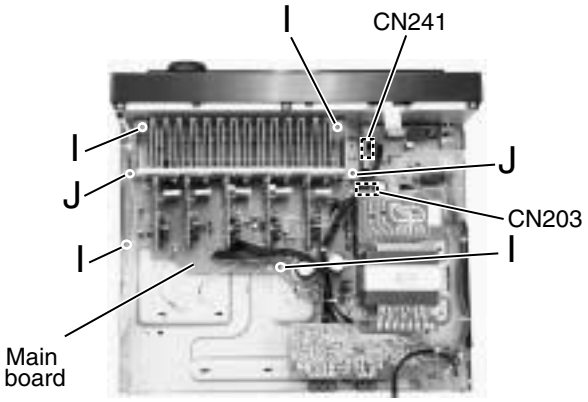


Fig.10

■Removing the Heat sink (See Fig.11 to 12)

1. Remove the ten screws K and four screws L attaching the heat sink.
2. Remove the two screws L' attaching the heat sink from the rear side of main board.

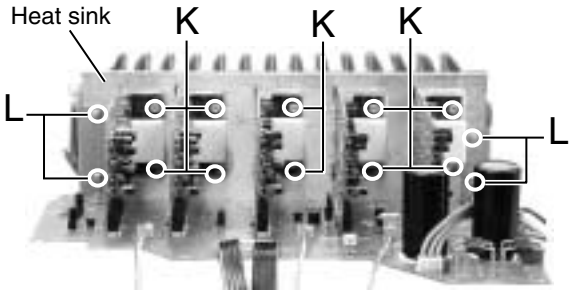


Fig.11

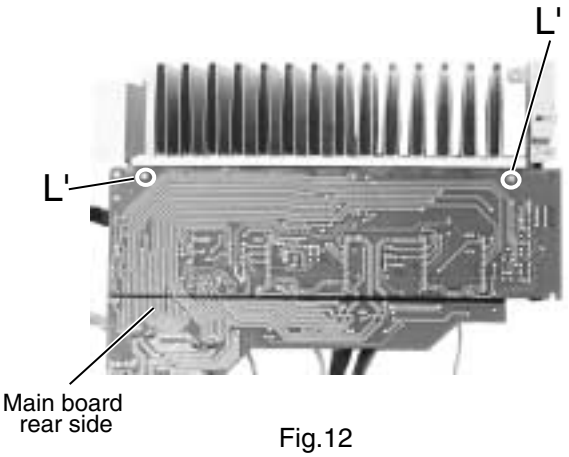


Fig.12

■ Removing the power transformer (See Fig.13)

・ Prior to performing the following procedures, remove the top cover.

1. Unsolder the two harnesses connected to the power transformer.
2. Disconnect the harness from connector CN251 and unsolder the harnesses connected to FW201 on the power transformer board.
3. Remove the four screws M attaching the power transformer.

■ Removing the power / fuse board (See Fig.13)

・ Prior to performing the following procedure, remove the top cover and the rear panel.

1. Remove the screw N attaching the power / fuse board.
2. Unsolder the power cord and other harnesses connected to the power / fuse board.

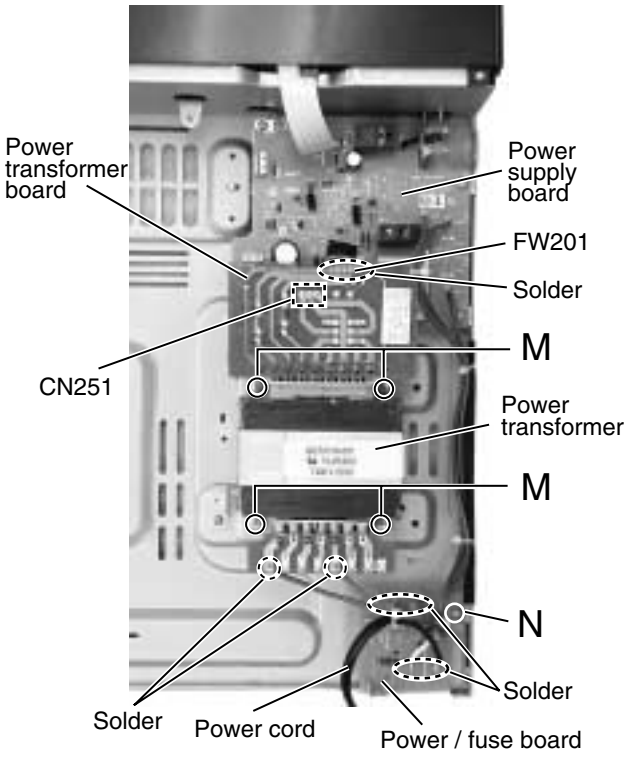


Fig.13

■ Removing the power supply board (See Fig.14 and 15)

・ Prior to performing the following procedure, remove the top cover and the front panel.

1. Remove the one nut attaching the headphone jack of the power supply board on the front side of the body.
2. Disconnect the harness connected to connector CN241,CN201,CN203 and CN291 on the power transformer board (If necessary, cut off the band fixing the harness on the side of the base chassis).
3. Remove the three screws O attaching the power supply board and pull out the power supply board from the front bracket backward.
4. Unsolder the three harnesses connected to the power supply board.

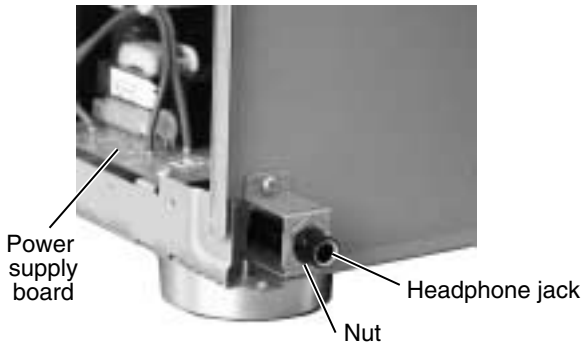


Fig.14

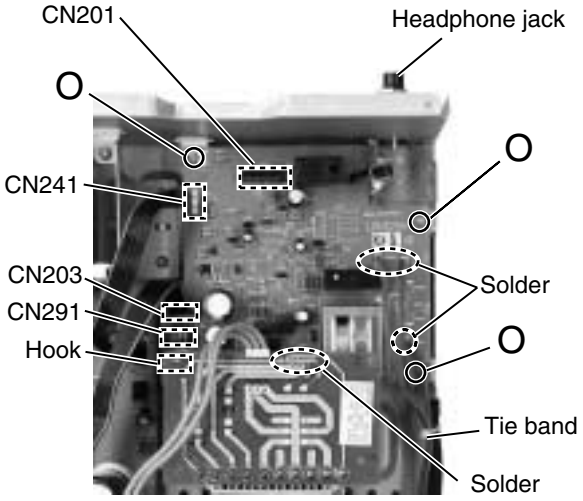


Fig.15

■Removing the system control board / power switch board (See Fig.16 to 18)

・ Prior to performing the following procedure, remove the top cover and the front panel assembly.

1. Pull out the volume knob on the front side of the front panel and remove the nut attaching the system control board.

2. Remove the two screws P attaching the power switch board.

3. Disconnect the harness from connector CN714 on the power switch board.

4. Remove the six screws Q attaching the system control board on the back of the front panel.

5. On the back of the front panel, release the eight joints by pushing the joint tabs inward.
   Remove the operation switch panel toward the front.

6. Release the two hook attaching the system control board.

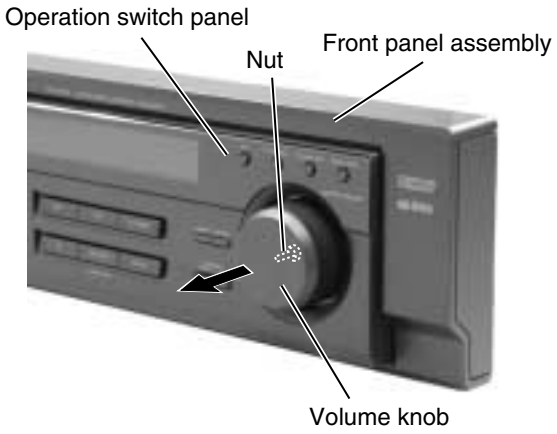


Fig.16

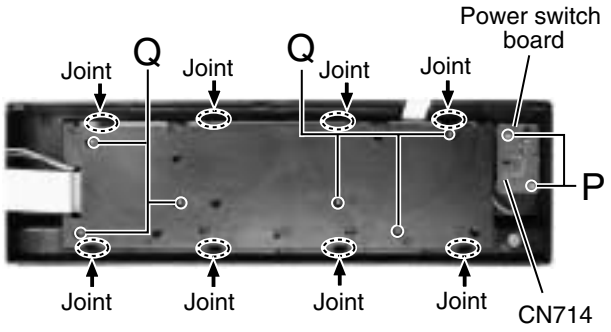


Fig.17

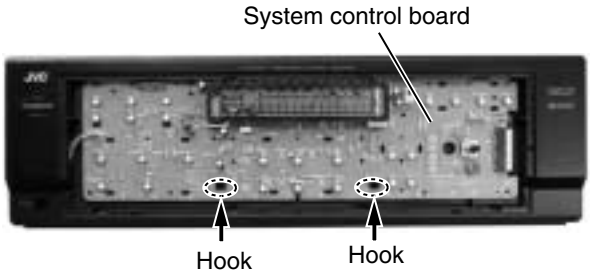


Fig.18

Adjustment method

■ Tuner section

1.Tuner range

FM		87.5MHz~108.0MHz
AM	(MW)	522kHz~1629kHz
	(LW)	144kHz~ 288kHz

■ Power amplifier section

Adjustment of idling current

Measurement location	TP301(Lch) , TP302(Rch)
Adjustment part	VR301(Lch) , VR302(Rch)

Attention
This adjustment does not obtain a correct adjustment value immediately after the amplifier is used (state that an internal temperature has risen).
Please adjust immediately after using the amplifier after turning off the power supply of the amplifier and falling an internal temperature.

<Adjustment method>

1.Set the volume control to minimum during this adjustment.(No signal & No load)

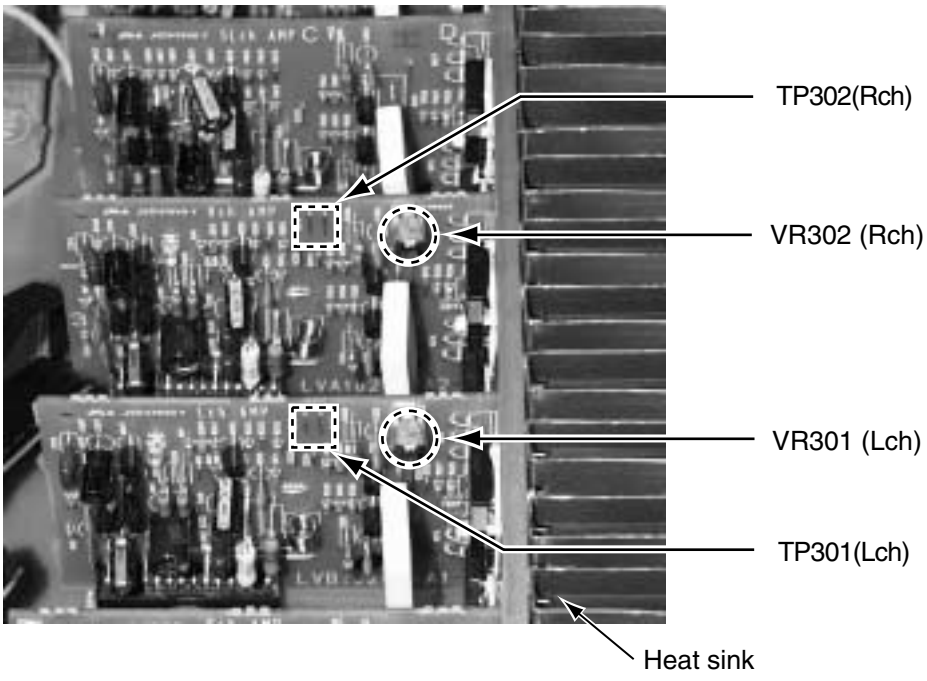
2.Set the surround mode OFF.

2.Turn VR301 and VR302 fully counterclockwise to warm up before adjustment.
If the heat sink is already warm from previous use the correct adjustment can not be made.

3.For L-ch,connect a DC voltmeter between TP301's B216 and B217 (Lch)
And,connect it between TP302's B218 and B219(Rch).

4.30 minutes later after power on, adjust VR301 for L-ch, or VR302 for R-ch so that the DC voltmeter value has 1mV~10mV.

* It is not abnormal though the idling current might not become 0mA even if it is finished to turn variable resistance (VR301,VR302) in the direction of counterclockwise.



Description of major ICs

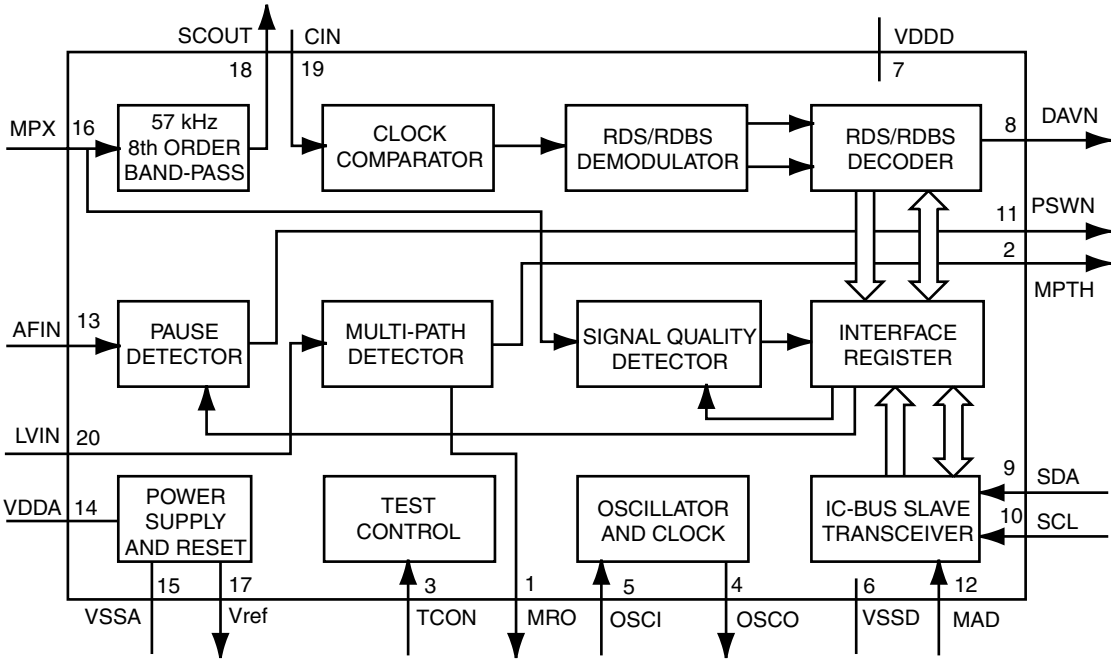
■ SAA6588 (IC191) : RDS detector

1.Terminal Layout

2.Pin Function

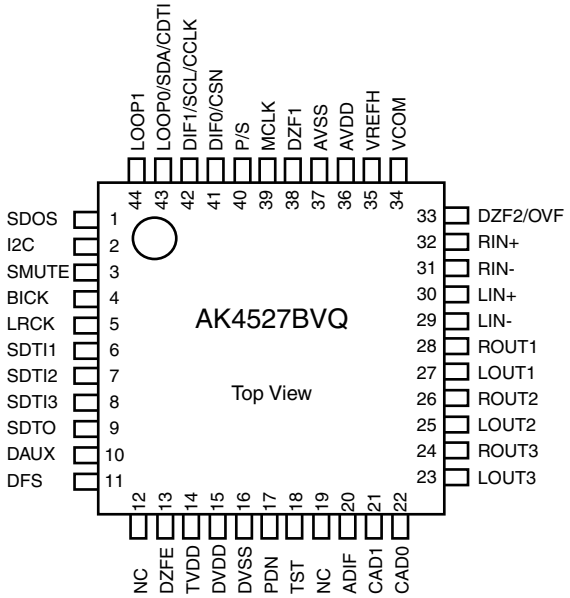
Pin No.	Symbol	I/O	Function
1	MRO	O	Multi-path rectifier output
2	NC	-	Non connect
3	GND	I	Test control input pin
4	OSCO	O	Oscillator output
5	OSCI	I	Oscillator input
6	VSSD	-	Digital ground (0V)
7	VDDD	-	Digital power supply (5V)
8	DAVN	O	Data available output (active LOW)
9	SDA	I/O	IC-bus serial data I/O
10	SCL	I	IC-bus serial clock input
11	NC	-	Non connect
12	GND	-	Connect to ground
13	NC	-	Non connect
14	VDDA	-	Analog power supply (5V)
15	VSSA	-	Connect to ground
16	MPX	I	Multiplex input signal
17	Vref	O	Reference voltage output
18	SCOUT	O	Band-pass filter output
19	CIN	O	Comparator output
20	NC	I	Level input

3.Block Diagram



■ AK4527B (IC601) : A/D,D/A converter

1.Pin layout



2. Pin function (1/2)

AK4527(1/2)

No.	Pin name	I/O	Function
1	SDOS	I	SDTO Source Select Pin (Note 1) "L" : Internal ADC output, "H" : DAUX input
2	I2C	I	Control Mode Select Pin "L" : 3-wire Serial, "H" : I2C Bus
3	SMUTE	I	Soft Mute Pin (Note 1) When this pin goes to "H", soft mute cycle is initialized. When returning to "L", the output mute releases.
4	BICK	I	Audio Serial Data Clock Pin
5	LRCK	I/O	Input Channel Clock Pin
6	SDTI1	I	DAC1 Audio Serial Data Input Pin
7	SDTI2	I	DAC2 Audio Serial Data Input Pin
8	SDTI3	I	DAC3 Audio Serial Data Input Pin
9	SDTO	O	Audio Serial Data Output Pin
10	DAUX	I	Sub Audio Serial Data Input Pin
11	DFS	I	Double Speed Sampling Mode Pin (Note 1) "L" : Normal Speed, "H" : Double Speed
12	NC	-	No Connect No internal bonding.
13	DZEF	I	Zero Input Detect Enable Pin "L" : mode 7 (disable) at parallel mode, zero detect mode is selectable by DZFM2-0 bits at serial mode. "H" : mode 0 (DZF is AND of all six channels)
14	TVDD	-	Output Buffer Power supply Pin, 2.7V~5.5V
15	DVDD	-	Digital Power Supply Pin, 4.5V~5.5V
16	DVSS	-	De-emphasis Pin, 0V
17	PDN	I	Power-Down & Reset Pin When "L", the AK4527B is powered-down and the control registers are reset to default state. If the state of P/S or CAD0-1 changes, then the AK4527B must be reset by PDN.
18	TST	I	Test Pin This pin should be connected to DVSS.

Pin function (2/2) AK4527(1/2)

No.	Pin name	I/O	No Connect Function
19	NC	-	No internal bonding.
			Analog Input Format Select Pin
20	ADIF	I	"H" : Full-differential input, "L" : Single-ended input
			Chip Address 1 Pin
21	CAD1	I	Chip Address 0 Pin
22	CAD0	I	DAC3 Lch Analog Output Pin
23	LOUT3	O	DAC3 Rch Analog Output Pin
24	ROUT3	O	DAC2 Lch Analog Output Pin
25	LOUT2	O	DAC2 Rch Analog Output Pin
26	ROUT2	O	DAC1 Lch Analog Output Pin
27	LOUT1	O	DAC1 Rch Analog Output Pin
28	ROUT1	O	Lch Analog Negative Input Pin
29	LIN-	I	Lch Analog Positive Input Pin
30	LIN+	I	Rch Analog Negative Input Pin
31	RIN-	I	Rch Analog Positive Input Pin
32	RIN+	I	Zero Input Detect 2 Pin (Note 2)
33	DZF2	O	When the input data of the group 1 follow total 8192LRCK cycles with "0" input data, this pin goes to "H".
			Analog Input Overflow Detect Pin (Note 3)
	OVF	O	This pin goes to "H" if the analog input of Lch or Rch is overflows.
			Common Voltage Output Pin,AVDD/2
34	VCOM	O	Large external capacitor around 2.2uF is used to reduce power-supply noise.
			Positive Voltage Reference Input Pin,AVDD
35	VREFH	I	Analog Power Supply Pin,4.5V~5.5V
36	AVDD	-	Analog Ground Pin,0V
37	AVSS	-	Zero Input Detect 1 Pin (Note 2)
38	DZF1	O	When the input data of the group 1 follow total 8192 LRCK cycles with "0" input data, this pin goes to "H".
			Master Clock Input Pin
39	MCLK	I	Parallel / Serial Select Pin
40	P/S	I	"L" : Serial control mode, "H" : Parallel control mode
			Audio Data Interface Format 0 Pin in parallel mode
41	DIF0	I	Chip select pin in 3-wire serial control mode
	CSN	I	This pin should be connected to DVDD at I2C bus control mode
			Audio Data Interface Format 1 Pin in parallel mode
42	DIF1	I	Control Data Clock Pin in serial control mode
	SCL/CCLK	I	I2C = "L" : CCLK(3-wire Serial), I2C = "H" : SCL(I2CBus)
			Loopback Mode 0 Pin in parallel control mode
43	LOOP0	I	Enables digital loop-back from ADC to 3 DACs.
			Control Data Input Pin in serial control mode
	SAD/CDTI	I/O	I2C = "L" : CDTI(3-wire Serial), I2C = "H" : SDA(I2CBus)
			Loopback Mode 1 Pin (Note 1)
44	LOOP1	I	Enable all 3 DAC channels to be input from SDTII.

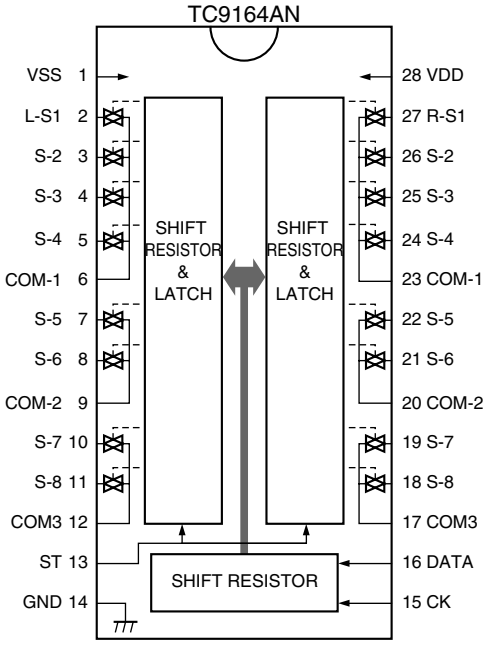
Notes : 1. SDOS, SMUTE, DFS, and LOOP1 pins are ORed with register data if P/S = "L".
2. The group 1 and 2 can be selected by DZFM2-0 bit if P/S = "L" and DZFME = "L".
3. This pin becomes OVF pin if OVFE bit is set to "1" at serial control mode.
4. All input pins should not be left floating.

■ TC9164AN (IC402) : Analog switch

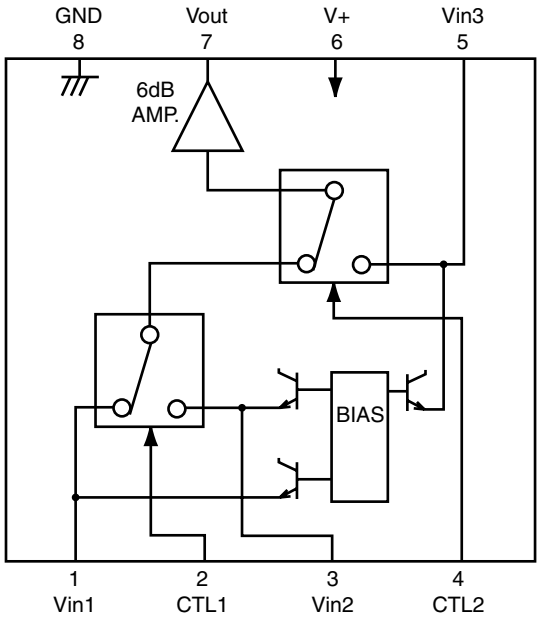
1.Function

Switch to On/Off of S1 to S8 by control of LSI.

2.Terminal Lay out & Block Diagram



■ NJM2246D (IC501) : Video switch

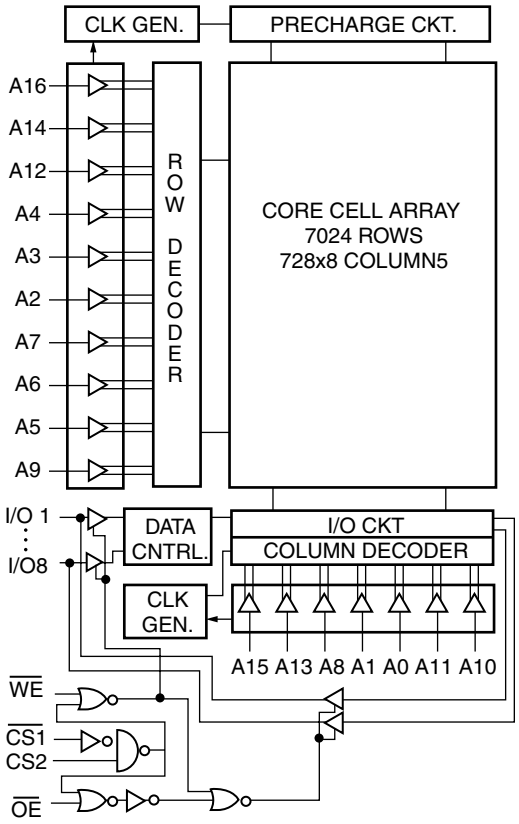


Control input - output signal

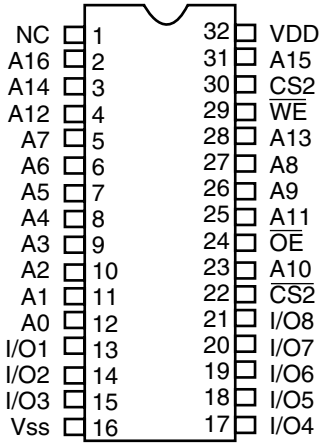
CTL 1	CTL 2	Output
L	L	VIN 1
H	L	VIN 2
L/H	H	VIN 3

■ W24L010AJ-12 (IC641) : CMOS SRAM

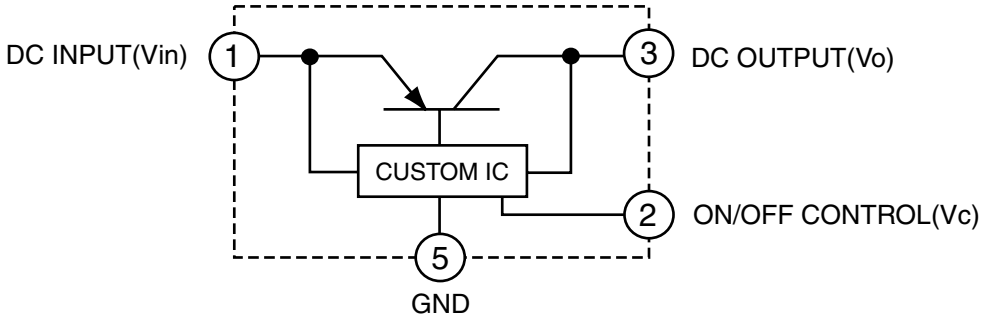
Block diagram



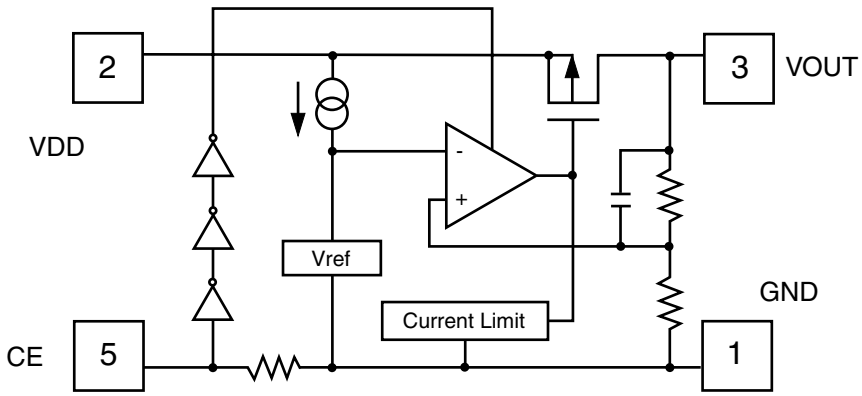
Pin layout



■ PQ3DZ53 (IC681) : Regulator IC

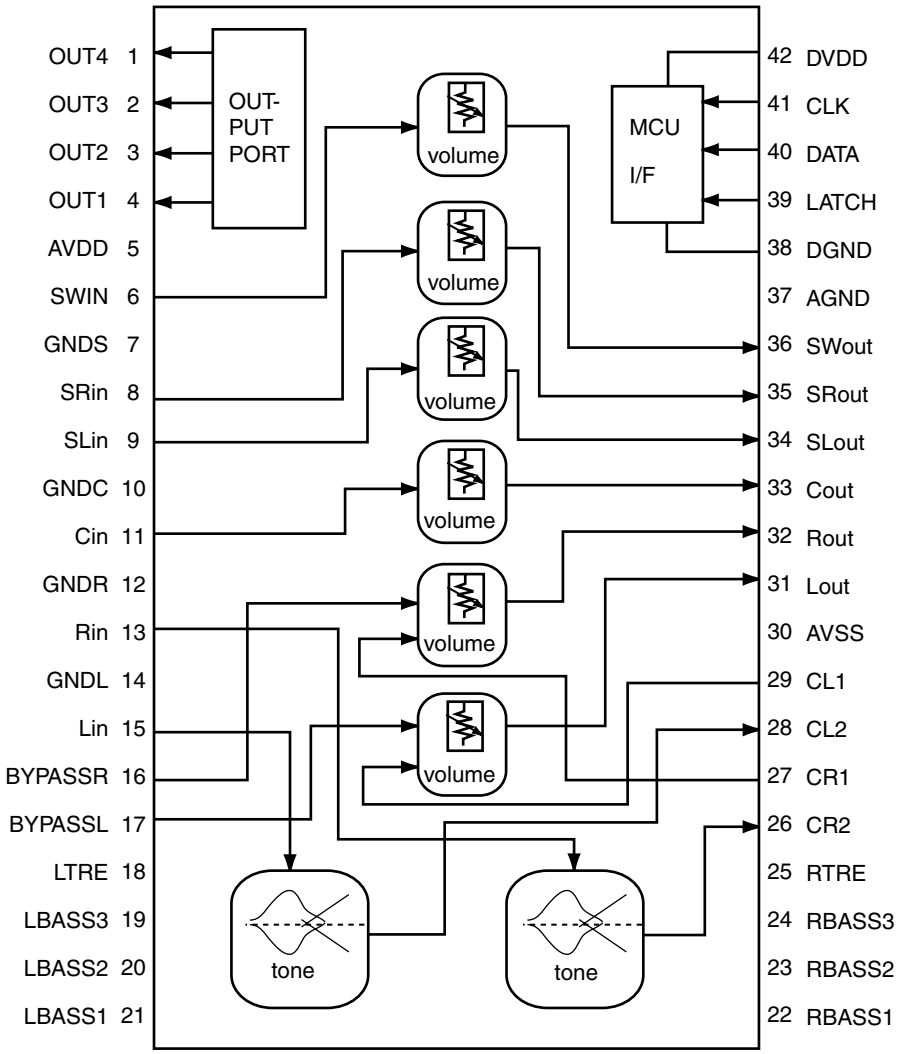


■ RN5RZ33BA (IC683) : Voltage regurator



■ M62446FP (IC428) : 6CH master volume

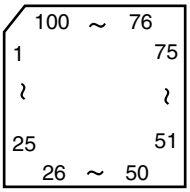
1.Block Diagram



2.Pin Function

Pin No.	Symbol	I/O	Descriptions
1	SURROUND	O	SURROUND control terminal
2	BASS BOOST	O	BASS BOOST control terminal
3	INPUT-ATT	O	Input attenuator control terminal
4	MUTING	O	MUTING control terminal
5	AVDD	-	Analog positive power supply terminal
6	SWIN	I	SUB Woofer volume signal input terminal
7	A.GND	-	Analog ground terminal
8	RR IN	I	R ch volume signal input terminal for rear speaker
9	RL IN	I	L ch volume signal input terminal for rear speaker
10	A.GND	-	Analog ground terminal
11	C IN	I	Center volume signal input terminal
12	A.GND	-	Analog ground terminal
13	R IN	I	R ch volume signal input terminal
14	A.GND	-	Analog ground terminal
15	L IN	I	L ch volume signal input terminal
16,17	BYPASSR,L	-	Non connect
18	LTRE	-	Frequency adjustment terminal tone/treble
19~21	LBASS3~1	-	Frequency adjustment terminal tone/bass
22	CR2	O	Tone output terminal
23,24	RBASS2,4	-	Frequency adjustment terminal tone/bass
25	RTRE	-	Frequency adjustment terminal tone/treble
26	RBASS1	-	Frequency adjustment terminal tone/bass
27	CR1	I	L/R volume input terminal
28	CL2	O	Tone output terminal
29	CL1	I	L/R volume input terminal
30	AVSS	-	Analog negative power supply terminal
31	L OUT	O	L ch output
32	R OUT	O	R ch output
33	C OUT	O	Center volume signal output terminal
34	RL OUT	O	L ch volume signal output terminal for rear speaker
35	RR OUT	O	R ch volume signal output terminal for rear speaker
36	SW OUT	O	SUB Woofer volume signal output terminal
37	A.GND	-	Analog ground terminal
38	D.GND	-	Digital ground terminal
39	VOL STB	I	Latch input terminal
40	VOL DATA	I	Volume data input terminal
41	VOL CLK	I	Clock input terminal for data transfer
42	DVDD	-	Digital power supply terminal

■MN101C35DHK1 (IC701) : System controller



Pin function (1/2)

Pin No.	Symbol	I/O	Function
1	TXD/SB00/P00	I	VOL.JOG IN_1
2	RXD/SBI0/P01	I	VOL.JOG IN_2
3	SBT0/P02	I/O	DATA (PLL)
4	SB01/P03	O	CLK (PLL)
5	SBI1/P04	O	CE (PLL)
6	SBT1/P05	I	VIDEO S/C DVD
7	BUZZER/P06	I	VIDEO S/C VCR
8	VDD	-	Power supply +5V
9,10	OSC1,2	I/O	OSC (8MHz)
11	VSS	-	GND
12	XI	I	GND
13	X0	O	OPEN
14	MMOD	I	GND
15	VREF-	-	GND
16	AN0/PA0	I	KEY INPUT 1 (7KEY)
17	AN1/PA1	I	KEY INPUT 2 (7KEY)
18	AN2/PA2	I	KEY INPUT 3 (7KEY)
19	AN3/PA3	I	KEY INPUT 4 (7KEY)
20	AN4/PA4	I	KEY INPUT 5 (7KEY)
21	AN5/PA5	I	INH IN
22	AN5/PA5	I	CHIP SELECT 1
23	AN5/PA5	I	CHIP SELECT 2
24	VREF+	-	Power supply +5V
25	P07	I	VIDEO S/C DBS
26	RST /P27	I	RESET INPUT
27	RNOUT/TM0I0/P10	O	RDS CLK OUT (RDS)
28	TM1I0/P11	I	DCS INPUT
29	TM2I0/P12	O	DCS OUTPUT
30	TM3I0/P13	I	AVLINK VCR IN
31	TM4I0/P14	O	AVLINK VCR OUT
32	P15	I/O	RDS DATA (RDS)
33	IRQ0/P20	I	PROTECTOR IN
34	SENS/IRQ1/P21	I	REMOCON INPUT
35	IRQ2/P22	I	TUNED IN (TUNER)
36	IRQ3/P23	I	STEREO IN (TUNER)
37	IRQ4/P24	I	RDS DAVN (RDS)
38	P25	I	SELF CHECK INPUT
39	SB02/P30	O	COMMAND (DSP)
40	SBI2/P31	I	STATUS (DSP)

Pin function (2/2)

Pin No.	Symbol	I/O	Function
41	SBT2/P32	O	CLK (DSP)
42	P50	O	READY (DSP)
43	P51	O	RESET (DSP)
44	P52	O	RELAY S
45	P53	O	RELAY C
46	P54	O	RELAY L/R 1
47	DGT17/P67	O	RELAY L/R 2
48	DGT16/P66	O	RELAY HEADPHONE
49～64	G16～G1	O	FL GRID SIGNAL CONTROL OUT
65～80	P87～P90	O	FL SEGMENT SIGNAL CONTROL OUT
81	SEG24/PC2	-	No Connect
82	SEG25/PC1	-	No Connect
83	SEG26/PC0	-	No Connect
84	SEG27/PB7	-	No Connect
85	SEG28/PB6	-	No Connect
86	SEG29/PB5	-	No Connect
87	SEG30/PB4	-	No Connect
88	SEG31/PB3	-	No Connect
89	SEG32/PB2	O	SOUSE MUTE
90	SEG33/PB1	O	SUBWOOFER MUTE
91	SEG34/PB0	O	TUNER MUTE
92	SEG35/PD7	O	POWER ON (STANDBY)
93	SEG36/PD6	O	SURROUND
94	SEG37/PD5	O	DATA (A.SW)
95	SEG38/PD4	O	CLK (A.SW)
96	SEG39/PD3	O	STB (A.SW)
97	SEG40/PD2	O	LATCH (VOL)
98	SEG41/PD1	O	DATA (VOL)
99	SEG42/PD0	O	CLK (VOL)
100	VPP	O	VPP

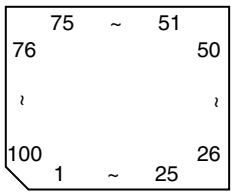
■ TC9446F-014 (IC631) : Digital signal processor for dolby digital (AC-3) / MPEG2 audio decode

Pin No.	Symbol	I/O	Function
1	$\overline{RST}$	I	Reset signal input terminal (L:reset H:Operation usually)
2	MIMD	I	Microcomputer interface mode selection input terminal (L:serial H:IC bus)
3	$\overline{MICS}$	I	Microcomputer interface chip select input terminal
4	$\overline{MILP}$	I	Microcomputer interface latch pulse input
5	MIDIO	I/O	Microcomputer interface data I/O terminal
6	$\overline{MICK}$	I	Microcomputer interface clock input terminal
7	MIACK	O	Microcomputer interface acknowledge output terminal
8~11	FI0~3	I	Flag input terminal 0~3
12	IRQ	I	Interrupt input terminal
13	VSS	-	Digital ground terminal
14	LRCKA	I	Audio interface LR clock input terminal A
15	BCKA	I	Audio interface bit clock input terminal A
16~18	SDO0~2	O	Audio interface data output terminal 0
19	SD03	-	Non connect
20	LRCKB	I	Audio interface LR clock input terminal B
21	BCKB	I	Audio interface bit clock input terminal B
22	SDT0	I	Audio interface data input terminal 0
23	SDT1	I	Audio interface data input terminal 1
24	VDD	-	Power supply for digital circuit
25	LRCKOA	O	Audio interface LR clock output terminal A
26	BCKOA	O	Audio interface bit clock output terminal A
27,28	$\overline{TEST0,1}$	I	Test input terminal 0/1 (L:test H:operation usually)
29~31	LRCKOB,BCKOB,TXO	-	Non connect
32,33	$\overline{TEST2,3}$	I	Test input terminal (L:test H:operation usually)
34	RX	I	SPDIF input terminal
35	VSS	-	Ground terminal for digital circuit
36	$\overline{TSTSUB0}$	I	Test sub input terminal 0 (L:test H:operation usually)
37	FCONT	O	VCO Frequency control output terminal
38,39	$\overline{TSTSUB1,TSTSUB2}$	I	Test sub input terminal 1,2 (L:test H:operation usually)
40	PDO	O	Phase error signal output terminal
41	VDDA	-	Power supply for analog circuit
42	PLON	I	Clock selection input terminal (L:external clock H:VCO clock)
43	AMPI	I	AMP.input terminal for LPF
44	AMPO	O	AMP.output terminal for LPF
45	CKI	I	External clock input terminal
46	VSSA	-	Ground terminal for analog circuit
47	CKO	O	DIR Clock output terminal
48	LOCK	O	VCO Lock detection output terminal
49	VSS	-	Ground terminal for digital circuit
50	$\overline{WR}$	O	External SRAM writing signal output terminal
51	$\overline{OE}$	O	External SRAM output enable signal output terminal
52	$\overline{CE}$	O	External SRAM chip enable signal output terminal
53	VDD	-	Power supply terminal for digital circuit
54~61	IO7~0	I/O	External SRAM data I/O terminal 7~0
62	VSS	-	Ground terminal for digital circuit
63~70	AD0~7	O	External SRAM address output terminal 0~7
71	VDD	-	Power supply terminal for digital circuit
72~80	AD8~16	O	External SRAM address output terminal 8~16
81	VSS	-	Ground terminal for digital circuit
82~89	PO0~7	O	General purpose output terminal 0~7
90	VDDDL	-	Power supply terminal for DLL
91	LPFO	O	LPF output terminal for DLL
92,93	DLON,DLCKS	I	Refer to the undermentioned table
94	SCKO	-	Non connect
95	VSSDL	-	Ground terminal for DLL
96	SCKI	I	External system clock input terminal
97	VSSX	-	Ground termonal for oscillation circuit
98,99	XO,XI	I/O	Oscillation I/O terminal
100	VDDX	-	Power supply terminal for oscillation circuit

DLCKS terminal	DLONterminal	DLL clock setting
L	L	SCKI input (DLL circuit OFF)
L	H	Four times XI clock
H	L	Three times XI clock
H	H	Six times XI clock

■ UPD784215AGC103 (IC671) : UNIT CPU

1.Pin layout



2.Pin function

Pin No.	Symbol	I/O	Function
1~8		-	Non connect
9	VDD	-	Power supply terminal
10	X2	O	Connecting the crystal oscillator for system main clock
11	X1	I	Connecting the crystal oscillator for system main clock
12	VSS	-	Connect to GND
13	XT2	O	Connecting the crystal oscillator for system sub clock
14	XT1	I	Connecting the crystal oscillator for system sub clock
15	$\overline{\text{RESET}}$	I	System reset signal input
16	$\overline{\text{AUTODATA}}$	I	Output of DSP to general-purpose port
17	LOCK	I	Output of DSP to general-purpose port
18	DIGITAL0	I	Output of DSP to general-purpose port
19	FORMAT	I	Output of DSP to general-purpose port
20	CHANNEL	I	Output of DSP to general-purpose port
21	ERR	I	Output of DSP to general-purpose port
22	$\overline{\text{RSTDET}}$	I	Reset signal input
23	AVDD	-	Power supply terminal
24	AVREF0	-	Connect to GND
25~32		-	Connect to GND
33	AVSS	-	Connect to GND
34,35		-	Non connect
36	AV REF1	-	Power supply terminal
37,38	RX,TX	-	Not use
39		-	Non connect
40	DSPCOM	I	Communication port from IC701
41	DSPSTS	O	Status communication port to IC701
42	$\overline{\text{DSPCLK}}$	I	Clock input from IC701
43	DSPRDY	I	Ready signal input from IC701
44		-	Non connect
45,46	MIDIO_IN/OUT	I/O	Interface I/O terminal with microcomputer
47	$\overline{\text{MICK}}$	O	Interface I/O terminal with microcomputer of clock signal
48	$\overline{\text{MICS}}$	O	Interface I/O terminal with microcomputer of chip select
49	$\overline{\text{MILP}}$	O	Interface I/O termonal with microcomputer
50	$\overline{\text{MIACK}}$	O	Interface I/O termonal with microcomputer
51,52		-	Non connect
53	$\overline{\text{DSPRST}}$	O	Reset signal output of DSP
54~63		-	Non connect
64,65	CDTI/CDTO	I/O	Interface I/O terminal with microcomputer
66	$\overline{\text{CCLK}}$	O	Interface I/O terminal with microcomputer of clock signal
67	$\overline{\text{CS}}$	O	Interface I/O terminal with microcomputer of chip select
68	XTS	O	OSC Select
69,70		-	Non connect
71	$\overline{\text{PD}}$	O	Reset signal output
72	GND	-	Connect to GND
73~80		-	Non connect
81	VDD	-	Power supply
82	$\overline{\text{3D-ON}}$	-	Non connect
83	3D-ON	O	Switch at output destination of surround channel
84	ANA/T-TONE	O	Test tone control
85	REF-MIX	O	Control at output destination of LFE channel
86		-	Non connect
87	D.MUTE	O	Mute of the digital out terminal is controlled
88	$\overline{\text{S.MUTE}}$	O	Mute of the audio signal is controlled
89		-	Non connect
90~93	ASW1~4	O	Selection of digital input selector
94	TEST	-	Test terminal
95~100		-	Non connect

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